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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/892,816	MCGREW ET AL.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 2, 2004 has been entered.

Response to Amendment

2. This Office Action is in responded to the amendment filed on July 9, 2004 (Paper No. 12).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-4, 14-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 14, and 18, recites the limitation "the memory". There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 23, recites the limitation "the separate memory" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Regarding claims 2-13, 15-17 and 19-20 are also rejected because of depending on claims 1, 14 and 18, respectively, containing the same deficiency.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. (US PAT. 5,590,306 hereinafter Watanabe).

Regarding claim 1, Watanabe discloses a method comprising receiving a request to download data, i.e., write command, into flash memory, i.e., IC memory (4, figure 1), halting the downloading of the data into the flash memory until the flash memory is initialized, i.e., memory card controller (1, figure 1) comprising main control circuit (18, figure 1), management information updating circuit (16, figure 1), management information read circuit (14, figure 1) and other processing elements, wherein the main control circuit is able to interrupt the writing data into the flash memory when the recording data is abnormal manner (col. 11 line 8 through col. 12 line 27), wherein the initialization includes storing pointers in a second memory to indicated different locations within the flash memory where the data is to be stored within the

flash memory, i.e., IC memory card comprising a supervisory area (30, figure 2), i.e., second memory, stores the management data relating to the data recording in the data unit (32, figure 2), wherein the supervisory area further comprising the classification/attribute information relating to the recording data, such as packet identification, i.e., pointer, (figure 3 and col. 8 line 53 through col. 9 line 67), and storing the data into the flash memory based on the pointers stored in the memory (col. 10 line 39 through col. 11 line 7 and col. 24 line 28 through col. 25 line 47).

Regarding claim 2, Watanabe disclosures the method wherein the initialization of the flash memory comprises generating headers for the different locations within the flash memory where the data is to be stored (figure 3 and col. 8 line 53 through col. 9 line 33), and storing the headers at the different locations, i.e., storing in the supervisory area (30, figure 2) with other management data (figure 3 and col. 8 line 53 through col. 9 line 33).

Regarding claim 4, Watanabe disclosures the method wherein the initialization of the flash memory comprises reclaiming space within the flash memory that is reclaimable for storage of data into the flash memory (col. 18 line 43-62 and col. 24 lines 18-27).

7. Claim 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Brown, III et al. (US PAT. 6,038,636 hereinafter Brown).

Regarding claim 5, Brown discloses a method comprising receiving a request, i.e., write or update request, from an external device, i.e., host computer (12, figure 1) to store data into a flash memory (20, figure 1) of a device (14, figure 1), wherein the request includes the size of the data, i.e., requesting data required number of data blocks in the flash memory as an example show in figure 2, file 1 contains data blocks (64, 66, 94 and 96), in response to receiving the

request, initializing the flash memory of device prior to receiving the data, wherein the initializing comprises determining whether the size of free space with the flash memory is greater than the size of the data, (col. 5 lines 1-67), and upon determining that the size of the free space within the flash memory is not greater than the size of the data, reclaiming space within the flash memory (col. 6 lines 1-29)

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US PAT. 5,590,306 hereinafter Watanabe).

Regarding claim 3, Watanabe disclosures the method further comprising storing the data received from the download into buffer (24, figure 2) prior to storing the data into the flash memory (col. 10 lines 1-63 and col. 21 lines 46-54). The difference between Watanabe and the claim is the claim specifically recite the storing data is download into a number of buffers. However, having a number of buffers does not have a disclosed purpose nor is this capacity disclosed to overcome any deficiencies in the prior art. As such, that could be only or any number of buffer. In addition, since Watanabe discloses the buffer (24, figure 2) is a static RAM having a storage capacity which is N times as much as the data area of the EEPRORM (32, figure 2), where N is a positive number (col. 10 lines 10-21), the ordinary artisan would realize a

possible buffer size increase as the current technology would warrant. Accordingly, it would have been an obvious matter of design choice to utilize the buffer of Watanabe wherein the size is disclosed above, furthermore, Watanabe disclosures the buffer (24, figure 2) is function to absorb the difference between the write rate of data into the storage unit and the transfer rate of data to be transferred from the IC memory card control device, which performs the same function as the claimed invention, since applicant has not disclosed that a buffer has such size and such functions, as opposed to other sizes, overcomes a deficiency in the prior art or is for any stated purpose.

10. Claims 6, 8-9, 22-23 and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown, III et al. (US PAT. 6,038,636 hereinafter Brown) in view of Watanabe et al. (US PAT. 5,590,306 hereinafter Watanabe).

Regarding claim 6, Brown disclosures the method further comprising generating headers for each of a number of different locations within the flash memory where the free space is located, storing the headers into the number of different locations within the flash memory (col. 7 line 17 through col. 9 line 33). Brown differs from the claimed invention in not specifically teaches the method further comprising storing pointers, in a separate memory, to the number of different location within the flash memory where the free space is located, transmitting a signal to the external device to transmit the data after the initialization of the flash memory is completed, receiving the data into a number of buffers within the device, and storing the data within the flash memory where the free space is located. However, Watanabe disclosures the IC memory card (4, figure 1), i.e., a device, comprising storage unit (20, figure 2), i.e., flash

memory, wherein the flash memory further comprising a supervisory data area (30, figure 2) and the data area (32, figure 2), the supervisory data area comprising the management information associated with the data in the data area, wherein the management information including bank packet identification, bank directory information, i.e., pointer, and bank memory allocation table information (col. 8 line 53 through col. 9 line 67 and col. 11 lines 7-28), the IC memory card further comprising card control unit (22, figure 2) coupled to storage unit (20) and memory controller (1, figure 1), i.e., external device via the connectors (3a and 3b), after the initialization of the flash memory is completed, i.e., completed checking the management information in memory (30), the card control unit (28) is transmitting a signal, i.e., ready signal (col. 14 line 1-32) to the external device, in addition, Watanabe teaches the memory card device (4) further comprising a buffer (24, figure 2), and storing the data (col. 10 lines 1-63 and col. 21 lines 46-54). Although Watanabe does not clearly teaches having a number of buffers in the device, however, having a number of buffers does not have a disclosed purpose nor is this capacity disclosed to overcome any deficiencies in the prior art. As such, that could be only or any number of buffer. In addition, since Watanabe discloses the buffer (24, figure 2) is a static RAM having a storage capacity which is N times as much as the data area of the EEPRORM (32, figure 2), where N is a positive number (col. 10 lines 10-21), the ordinary artisan would realize a possible buffer size increase as the current technology would warrant. Accordingly, it would have been an obvious matter of design choice to utilize the buffer of Watanabe wherein the size is disclosed above, furthermore, Watanabe disclosures the buffer (24, figure 2) is function to absorb the difference between the write rate of data into the storage unit and the transfer rate of data to be transferred from the IC memory card control device, which performs the same

function as the claimed invention, since applicant has not disclosed that a buffer has such size and such functions, as opposed to other sizes, overcomes a deficiency in the prior art or is for any stated purpose. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory system of Brown in having a method of storing pointers, in a separate memory, to the number of different location within the flash memory where the free space is located, transmitting a signal to the external device to transmit the data after the initialization of the flash memory is completed, receiving the data into a number of buffers within the device, and storing the data within the flash memory where the free space is located, as per teaching by the memory card system of Watanabe, because it efficiently utilize the storage capacity of the memory device and preventing data of the defective packets from being read out.

Regarding claim 8, Brown disclosures the method further comprising disabling interrupts within the device when potions of the data are being writing into the number of different locations in the flash memory, i.e., the flash memory in the printer is able to determine whether the size of the downloading data, and perform restoration and de-fragmentation process (col. 5 lines 55-67).

Regarding claim 9, Watanabe disclosures the method further comprising determining whether interrupts are pending in the device periodically during time the data is being written into the number of different locations in the flash memory, and periodically halting the writing of the data into the number of different locations in the flash memory and servicing the interrupts that are pending the device upon determining that interrupts are pending (col. 11 line 30 through col. 12 line 27, col. 14 lines 11-32 and figure 17b case 3).

Regarding claim 22, Brown discloses a machine readable medium that provides instructions which when executed by a machine, i.e., host computer (12, figure 1), causes the machine to perform operations comprising receiving a request, i.e., write or update request, from an external device, i.e., host computer (12, figure 1) to store data into a flash memory (20, figure 1) of a device (14, figure 1), wherein the request includes the size of the data, i.e., requesting data required number of data blocks in the flash memory as an example show in figure 2, file 1 contains data blocks (64, 66, 94 and 96), in response to receiving the request, initializing the flash memory of device prior to receiving the data, wherein the initializing comprises determining whether the size of free space with the flash memory is greater than the size of the data, (col. 5 lines 1-67), and upon determining that the size of the free space within the flash memory is not greater than the size of the data, reclaiming space within the flash memory (col. 6 lines 1-29), in addition, Brown further teaches generating headers for each of a number of different locations within the flash memory where the free space is located, storing the headers into the number of different locations within the flash memory (col. 7 line 17 through col. 9 line 33). Brown differs from the claimed invention in not specifically teaches the method further comprising storing pointers, in a separate memory, to the number of different location within the flash memory where the free space is located, transmitting a signal to the external device to transmit the data after the initialization of the flash memory is completed, receiving the data into a number of buffers within the device, and storing the data within the flash memory where the free space is located. However, Watanabe disclosures the IC memory card (4, figure 1), i.e., a device, comprising storage unit (20, figure 2), i.e., flash memory, wherein the flash memory further comprising a supervisory data area (30, figure 2) and the data area (32, figure 2), the

supervisory data area comprising the management information associated with the data in the data area, wherein the management information including bank packet identification, bank directory information, i.e., pointer, and bank memory allocation table information (col. 8 line 53 through col. 9 line 67 and col. 11 lines 7-28), the IC memory card further comprising card control unit (22, figure 2) coupled to storage unit (20) and memory controller (1, figure 1), i.e., external device via the connectors (3a and 3b), after the initialization of the flash memory is completed, i.e., completed checking the management information in memory (30), the card control unit (28) is transmitting a signal, i.e., ready signal (col. 14 line 1-32) to the external device, in addition, Watanabe teaches the memory card device (4) further comprising a buffer (24, figure 2), and storing the data (col. 10 lines 1-63 and col. 21 lines 46-54). Although Watanabe does not clearly teaches having a number of buffers in the device, however, having a number of buffers does not have a disclosed purpose nor is this capacity disclosed to overcome any deficiencies in the prior art. As such, that could be only or any number of buffer. In addition, since Watanabe discloses the buffer (24, figure 2) is a static RAM having a storage capacity which is N times as much as the data area of the EEPRORM (32, figure 2), where N is a positive number (col. 10 lines 10-21), the ordinary artisan would realize a possible buffer size increase as the current technology would warrant. Accordingly, it would have been an obvious matter of design choice to utilize the buffer of Watanabe wherein the size is disclosed above, furthermore, Watanabe disclosures the buffer (24, figure 2) is function to absorb the difference between the write rate of data into the storage unit and the transfer rate of data to be transferred from the IC memory card control device, which performs the same function as the claimed invention, since applicant has not disclosed that a buffer has such size and such functions, as

opposed to other sizes, overcomes a deficiency in the prior art or is for any stated purpose. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory system of Brown in having a method of storing pointers, in a separate memory, to the number of different location within the flash memory where the free space is located, transmitting a signal to the external device to transmit the data after the initialization of the flash memory is completed, receiving the data into a number of buffers within the device, and storing the data within the flash memory where the free space is located, as per teaching by the memory card system of Watanabe, because it efficiently utilize the storage capacity of the memory device and preventing data of the defective packets from being read out.

Regarding claim 23, Brown teaches the machine-readable medium wherein the separate memory is a random access memory (24, figure 2).

Regarding claim 25, the limitations of the claim are rejected as the same reasons set forth in claim 8.

Regarding claim 26, the limitations of the claim are rejected as the same reasons set forth in claim 9.

11. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US PAT. 5,590,306 hereinafter Watanabe) in view of Brown, III et al. (US PAT. 6,038,636 hereinafter Brown).

Regarding claim 10, Watanabe disclosure an apparatus comprising a flash memory (32, figure 2) in the IC memory card partitioned into blocks, i.e., cluster, (col. 8 line 59 through col. 9

line 5), a memory (30, figure 2) coupled to the flash memory, a write unit (22, figure 2) couple to the flash memory and the memory, wherein the write unit is to receive a request to download data into the flash memory, i.e., card control unit (22) receives the write request from the IC memory card controller (1, figure 1) via the connectors (3a and 3b) and (col. 8 lines 47-58), and wherein the write unit is to download the data into the flash memory, i.e., card control unit is able to transfer data and control signal to the storage unit (20, figure 2) via buses (204 and 206, figure 2) based upon the write request mode generated from the mode control (26, figure 2) in the card control unit (col. 10 line 22 through col. 11 line 7), and an initialize unit (28, figure) coupled to the flash memory, the memory and the write unit to initialize the flash memory in response to receiving the request to download data by storing pointers, prior to downloading the data into the flash memory (col. 10 line 39 through col. 11 line 7, figure 6 and col. 12 line 55 through col. 14 line 32), in the memory to indicate the number of the blocks within the flash memory that are free to store the data, i.e., the memory (30, figure 2) storing the management information associated with the data stored in the flash memory (32, figure 2), wherein the management information comprising card attribute information, bank header information, bank packet identification, and memory allocation table information, further, Watanabe disclosures each packet in the management information comprising binary code to indicated whether the related cluster is occupied to defined the available space in the flash memory corresponding to the memory allocation table information (col. 8 line53 through col. 9 line 67). Watanabe differs from the claimed invention in not specifically teaches the memory is a random access memory. However, Brown, teaches the printer comprising a flash memory (20, figure 1), an external random access memory (24, figure 1) under controlled of the printer control firmware (18, figure

1), wherein the external ram is able to store the header information corresponding to the bit map to specify each file block in the flash memory (col. 6 lines 30-37 and figures 5a and 5b). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory in the system of Watanabe is a random access memory, as per teaching of Brown, because both two memories are corresponding to their flash memory and performing to the similar function that storing management information and efficiently utilize the storage capacity and increase the memory accessing operation.

Regarding claim 11, Watanabe disclosures the initialize unit is to store headers at the number of different blocks within the flash memory, prior to downloading the data into the flash memory (figure 3 and col. 8 line 53 through col. 9 line 33).

Regarding claim 12, Brown disclosure the initialize unit is to reclaim space, prior to downloading the data into the flash memory, within the flash memory that is reclaimable for storage of the data into the flash memory upon determining that the size of free space within the flash memory is less than the size of the data to be downloaded into the flash memory (col. 5 lines 18-67).

Regarding claim 13, Watanabe disclosures the method further comprising storing the data received from the download into buffer (24, figure 2) prior to storing the data into the flash memory (col. 10 lines 1-63 and col. 21 lines 46-54). The difference between Watanabe and the claim is the claim specifically recite the storing data is download into a number of buffers. However, having a number of buffers does not have a disclosed purpose nor is this capacity disclosed to overcome any deficiencies in the prior art. As such, that could be only or any number of buffer. In addition, since Watanabe discloses the buffer (24, figure 2) is a static RAM

having a storage capacity which is N times as much as the data area of the EEPRORM (32, figure 2), where N is a positive number (col. 10 lines 10-21), the ordinary artisan would realize a possible buffer size increase as the current technology would warrant. Accordingly, it would have been an obvious matter of design choice to utilize the buffer of Watanabe wherein the size is disclosed above, furthermore, Watanabe disclosures the buffer (24, figure 2) is function to absorb the difference between the write rate of data into the storage unit and the transfer rate of data to be transferred from the IC memory card control device, which performs the same function as the claimed invention, since applicant has not disclosed that a buffer has such size and such functions, as opposed to other sizes, overcomes a deficiency in the prior art or is for any stated purpose.

12. Claims 14-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al. (US PAT. 6,791,877 hereinafter Miura) in view of Watanabe et al. (US PAT. 5,590,306).

Regarding claim 14, Miura disclosures a cellular phone uses the memory module wherein the cellular phone comprising a processor and a memory module wherein the memory module further comprising a DRAM and a flash memory which stores a basic program and application programs, and the processor executes the instruction which downloaded in the DRAM and flash memory, and the processor further downloading data from the Web browser, i.e., sever, via the wireless block RF, base upon the user requested (figure 45 and col. 42 line 16 through col. 43 line 11), in addition, Miura further disclosures, the flash memory in the memory module is partitioned into blocks (figure 3 and col. 10 lines 10-21). Miura differs from the claimed invention in not specifically teaches the processor further halt the downloading of the data into

the flash memory until the flash memory is initialized, wherein the initialization includes storing pointers in the random access memory to indicated the number of the blocks within the flash memory where the data is to be stored, and stored the data into the flash memory based on the pointers stored in the memory. However, Watanabe discloses a method comprising receiving a request to download data, i.e., write command, into flash memory, i.e., IC memory (4, figure 1), halting the downloading of the data into the flash memory until the flash memory is initialized, i.e., memory card controller (1, figure 1) comprising main control circuit (18, figure 1), management information updating circuit (16, figure 1), management information read circuit (14, figure 1) and other processing elements, wherein the main control circuit is able to interrupt the writing data into the flash memory when the recording data is abnormal manner (col. 11 line 8 through col. 12 line 27), wherein the initialization includes storing pointers in a second memory to indicated different locations within the flash memory where the data is to be stored within the flash memory, i.e., IC memory card comprising a supervisory area (30, figure 2), i.e., second memory, stores the management data relating to the data recording in the data unit (32, figure 2), wherein the supervisory area further comprising the classification/attribute information relating to the recording data, such as packet identification, i.e., pointer, (figure 3 and col. 8 line 53 through col. 9 line 67), and storing the data into the flash memory based on the pointers stored in the memory (col. 10 line 39 through col. 11 line 7 and col. 24 line 28 through col. 25 line 47). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the processor is capable to halt the downloading of the data into the flash memory until the flash memory is initialized, wherein the initialization includes storing pointers in the random access memory to indicated the number of the blocks within the flash

memory where the data is to be stored, and stored the data into the flash memory based on the pointers stored in the memory, as per teaching by Watanabe, because it efficiently utilize the storage capacity of the memory device and preventing data of the defective packets from being read out.

Regarding claim 15, Watanabe disclosures the method wherein the initialization of the flash memory comprises generating headers for the different locations within the flash memory where the data is to be stored (figure 3 and col. 8 line 53 through col. 9 line 33), and storing the headers at the different locations, i.e., storing in the supervisory area (30, figure 2) with other management data (figure 3 and col. 8 line 53 through col. 9 line 33).

Regarding claim 16, Watanabe disclosures the method further comprising storing the data received from the download into buffer (24, figure 2) prior to storing the data into the flash memory (col. 10 lines 1-63 and col. 21 lines 46-54). The difference between Watanabe and the claim is the claim specifically recite the storing data is download into a number of buffers. However, having a number of buffers does not have a disclosed purpose nor is this capacity disclosed to overcome any deficiencies in the prior art. As such, that could be only or any number of buffer. In addition, since Watanabe discloses the buffer (24, figure 2) is a static RAM having a storage capacity which is N times as much as the data area of the EEPRORM (32, figure 2), where N is a positive number (col. 10 lines 10-21), the ordinary artisan would realize a possible buffer size increase as the current technology would warrant. Accordingly, it would have been an obvious matter of design choice to utilize the buffer of Watanabe wherein the size is disclosed above, furthermore, Watanabe disclosures the buffer (24, figure 2) is function to absorb the difference between the write rate of data into the storage unit and the transfer rate of

data to be transferred from the IC memory card control device, which performs the same function as the claimed invention, since applicant has not disclosed that a buffer has such size and such functions, as opposed to other sizes, overcomes a deficiency in the prior art or is for any stated purpose.

Regarding claim 17, Watanabe disclosures the method wherein the initialization of the flash memory comprises reclaiming space within the flash memory that is reclaimable for storage of data into the flash memory (col. 18 line 43-62 and col. 24 lines 18-27).

Regarding claim 18, the limitations of the claim are rejected as the same reasons set forth in claim 14.

Regarding claim 19, the limitations of the claim are rejected as the same reasons set forth in claim 15.

Regarding claim 20, the limitations of the claim are rejected as the same reasons set forth in claim 16.

Regarding claim 21, the limitations of the claim are rejected as the same reasons set forth in claim 17.

13. Claims 7 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown, III et al. (US PAT. 6,038,636 hereinafter Brown) and Watanabe et al. (US PAT. 5,590,306) further in view of over Miura et al. (US PAT. 6,791,877 hereinafter Miura).

Regarding claim 7, the combination of Brown and Watanabe differs from the claimed invention in not specifically teaches the device is a cellular telephone and the external device is a server coupled to a network and wherein the data is transmitted to the cellular telephone through

a wireless transmission link. However, Miura teaches a cellular phone uses the memory module wherein the cellular phone comprising a processor and a memory module wherein the memory module further comprising a DRAM and a flash memory which stores a basic program and application programs, and the processor executes the instruction which downloaded in the DRAM and flash memory, and the processor further downloading data from the Web browser, i.e., sever, via the wireless block RF, base upon the user requested (figure 45 and col. 42 line 16 through col. 43 line 11). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Brown and Watanabe in having a device is a cellular telephone and the external device is a server coupled to a network and wherein the data is transmitted to the cellular telephone through a wireless transmission link, as per teaching by the cellular phone system of Miura, because it improves the reliability of downloading audio and video data from the website to the cellular phone.

Regarding claim 24, the limitations of the claim are rejected as the same reasons set forth in claim 7.

Response to Arguments

14. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Konishi et al. (US PAT. 5,579,502) disclosures memory card apparatus using EEPROMs For buffering data transfer between the EEPROMs and an external device (abstract).

Basentsch et al. (US PAT. 6,272,607) disclosures method and apparatus for transactional writing of data into a persistent memory (abstract).

Chang et al. (US PAT. 6,754,765) disclosures flash memory controller with updateable microcode (col. 2 line 33 through col. 3 line 60).

Asnaashari (US PAT. 6,076,137) disclosures method and apparatus for storing location identification information within non-volatile memory device (col. 3 line 34 through col. 4 line 40).

Spiegel et al. (US PAT. 6,571,326) disclosures space allocation for data in a non-volatile memory wherein reserve for a data write, so sufficient unallocated space can be confirmed as available for the write prior to actually writing the data to the nonvolatile memory (abstract and figure 4).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tue-Fri 8:00 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

17. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

October 29, 2004